

Design and performance of the readout system of the MINOS Far Detector

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Abstract—The MINOS experiment is a long baseline search for neutrino oscillations in an intense neutrino beam produced at Fermilab. This beam is intercepted by two detectors; the Near Detector at Fermilab and the Far Detector located a distance of 735 km in a mine in Soudan, Minnesota. The Far Detector is an iron / scintillator tracking calorimeter comprising some 185,000 channels of optical fibers read out by multi-anode photomultiplier tubes. As of this writing, the MINOS Far Detector has been completely installed and instrumented with a readout system. The readout system, along with performance measurements, will be presented.

Index Terms—MINOS, Far Detector, readout, neutrino oscillation

I. INTRODUCTION

THE MINOS Far Detector^[1] is a 5,400 metric ton tracking calorimeter composed of magnetized steel planes which are read out by a system of scintillator bars, wavelength shifting fibers, and 16-anode photomultiplier tubes. The detector operates in a mine in Soudan, Minnesota, at a depth of approximately 700 m. The readout system is highly multiplexed and hierarchical, specifically designed to take advantage of the low background rates in the underground environment while providing high dynamic range to track muons and measure hadronic showers. Each wavelength shifting fiber is read out at both ends, resulting in an optical channel count of approximately 185,000. The fibers are “multiplexed” onto the PMT pixels, which is to say, eight fibers at each end are connected to a single pixel, with the fiber-to-pixel mapping different at each end. This scheme enables the determination of correct track location with an eight-fold reduction in pixels.

The front end board integrates charge from 16 anodes in each of 3 PMTs and produces triggers based on charge collected by a common dynode. A single VME readout and digitizer card collects and processes data from up to 12 front end cards over approximately eight meters of cable and passes data to the VME bus. Thus, one readout card services 36 PMTs or 576 pixels for a highly compact readout system as shown in Fig. 1.

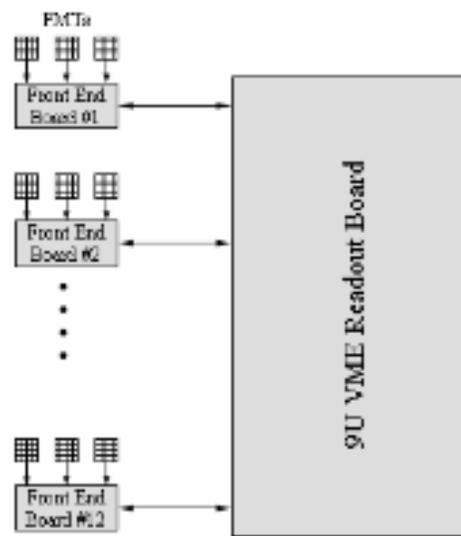


Fig. 1 Readout architecture

II. READOUT REQUIREMENTS

Dynamic range requirement is estimated as follows. In order to get good efficiency for accepting single photoelectrons, we need to set a threshold of 1/3 pe. The noise level, in turn, must be 1/3 of the threshold or 1/9 pe. In order to provide calorimetric energy measurement of hadron shower, we require signals of up to 175 pe be in the linear range. Ignoring pixel gain variations, this would imply dynamic range requirement of 1,575:1. Pixel gain variations for the M16 PMTs (Hamamatsu) are of order 3:1 thus bringing the dynamic range requirement up to ~ 4700:1 or just over 12 bits.

The expected singles rates from the PMTs are of order 1kHz per tube and the readout architecture must handle this rate with a dead time of no worse than ~1% or so. Triggers are generated by means of the final dynode of the PMT. This dynode is common to all anodes and delivers approximately half the charge of a single anode. Trigger thresholds must be settable at the level of approximately 0.3 pe at the lowest pixel gain.

III. FRONT END CARD - VFB

The front end card, called VFB (VA Frontend Board) is based on the widely used VA or Viking chip from IDE Corp. Oslo, Norway. The version used in MINOS is the VA32-HDR11, derived from the VA32_HDR2, a high dynamic range standard device from IDE. It consists of 32 channels of preamp-integrators, sample/hold circuits, and an analog output multiplexer controlled by a shift register. Detailed information can be found on the IDE web site. Three of these chips are used on each VFB as shown in Fig. 2. While a 16 channel chip would have sufficed for the 16 anode PMT, the savings in silicon would not have warranted the additional design expense. Four of the additional channels of each chip, in any case, are used for common mode noise suppression.

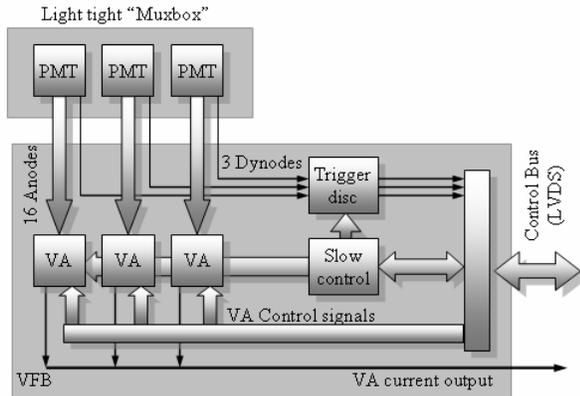


Fig. 2 VA Front End Board (VFB)

Trigger pulses are formed by an ASD-lite [2] chip, which is a four channel Amp/Shaper/Discriminator and a pre-cursor to the octal MDT-ASD [3] used in the Muon Spectrometer. The VFB is a slave readout board and has no on-board intelligence. Low level trigger pulses from single photoelectrons are sent off-board where trigger decisions are made. A simple serial interface is used to enable remote setup of bias voltages and currents needed to set up the VA and ASD-lite chips. Trigger pulses, slow control, and VA readout control signals share a common LVDS control bus. The VA analog outputs are differential current signals and share a common low dispersion shielded twisted pair cable[4] to the readout board.

IV. READOUT BOARD – VARC

The readout board, or VARC (VA Readout Controller), handles up to 12 VFBs and is shown in Fig. 3

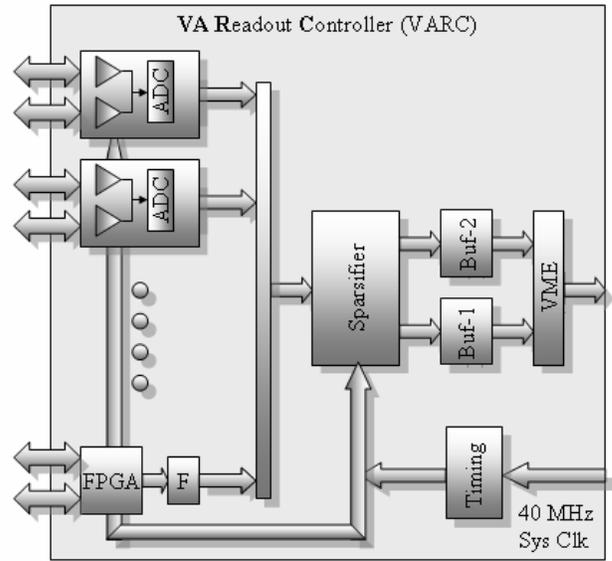


Fig. 3 VA Readout Controller (VARC)

The board's front end contains six identical sections, each of which services two VFBs. A pair of common base receivers, a 2:1 multiplexer, and a 14-bit, 10 Ms/sec ADC [5] are mounted on mezzanine cards called VMMs (VARC Mezzanine Modules, shown in upper two sections only). Each VMM has on-board voltage regulators to insure power isolation from the digital circuits below. Each of the six sections also contains an FPGA[6] controller and a data fifo mounted directly on the VARC beneath the mezzanine cards and shown in the lower section of the diagram. The VFB's control cables mount directly to the VARC while the analog data cable plugs into the VMM.

On receipt of a trigger from one of the six associated PMTs, the FPGA controller initiates a readout sequence of all 16 anode channels and four additional empty cells in the VA chip. The average value of these four empty channels will be subtracted from each anode channels pulse height for purposes of common mode noise suppression. This compensates for small drifts due to temperature variation and residual noise pickup in the VFBs and results in an overall reduction in pedestal width of the system.

A. Time stamping

Each trigger is time-stamped using a TDC implemented within the FPGA using its internal delay locked loops (DLLs). One DLL is used to double the 40 MHz system clock to 80 MHz, while a second generates four clock phases separated by 3.125 ns. Each trigger signal is registered by all four phases, thus timestamping the trigger in 3.125 ns bins. Two such circuits are used for each trigger, each separated by an external 1.5 ns passive delay. This effectively creates ~1.56 ns bins required to distinguish upward from downward going muons in the detector.

B. Data packets

Each dynode trigger results in a data packet which includes header information, 16 channels of PMT anode data, 4

channels of common mode VA data, and a timestamp. These data are placed into the data fifo for later readout.

C. Dead time

The VA readout process, including digitization, takes approximately 6 μ s to 10 μ s and during this time, triggers from the other 5 PMTs serviced by that controller may be received. If so, the Sample/Hold line on the associated VA chip is activated and the readout sequence is placed in a queue for later readout. Thus, no additional deadtime is incurred. At a 1kHz trigger rate per PMT, the system deadtime is thus \sim 1%.

On initial installation of the electronics on the MINOS Far Detector, an anomalously high trigger rate of the order of 5 kHz per PMT was observed. This was later traced to photons generated in the wavelength shifting fibers due to mechanical stress. This anomalous trigger rate was reduced using a 2 of 36 coincidence requirement implemented by firmware changes in the controller and spare communication lines between the FPGAs. This coincidence scheme resulted in a five to ten fold reduction in uncorrelated triggers and very low dead time.

D. Sparsification

The Sparsifier, implemented in an FPGA, reads data packets from the fifos in a round-robin fashion. The Sparsifier addresses two blocks of memory, corresponding to average pedestals and threshold values for each pixel. On processing a data packet, the pedestals are subtracted on a pixel by pixel basis, and each pixel is sparsified according to a threshold stored in memory. Thus pixel gain variations across the PMTs may be calibrated out and removed. Generally, the Sparsifier passes only one or a small number of pixels in each packet.

Data from the Sparsifier are packed into buffer memories for VME readout in ping-pong fashion. Timing is controlled by an external timing system and typically, each buffer stores 50 ms of data as the other is read out by VME in D32 transfers.

V. PERFORMANCE

The installation of the MINOS far detector was completed in July 2003 and has been taking cosmic ray data since installation began in the summer of 2001. The readout system has been stable and has performed as expected.

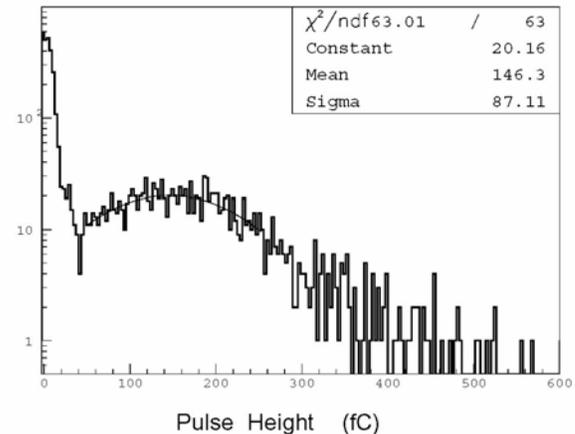


Fig. 4 Single photo-electron peak

Fig. 4 shows the unsparisified pulse height distribution for a single photoelectron. The single photoelectron peak is clearly visible with a nominal mean of 160 fC, while the pedestal, centered about zero, has an RMS of 6 fC, or 4% of the single photoelectron mean. The VA chip typically saturates at approximately 28 pC for a signal to noise ratio of 4700:1 (equivalent to 12.2 bits).

The readout system has exhibited good stability. Using the pulse height from cosmic ray muons, we have found that the average total gain, including photomultiplier tubes and readout electronics, does not vary by more than 1% over the course of several months. The mine environment in which the far detector is located is extremely stable, with the ambient temperature changing by at most 1 degree C, and contributes to the stability of the readout system.

Timing resolution has been studied as a function of pulseheight and results are shown in Fig. 5. The wavelength shifting fiber which transports scintillator light to the PMTs dominates the resolution at low pulse height. At large pulse height the timing resolution is seen to be 1.25 ns.

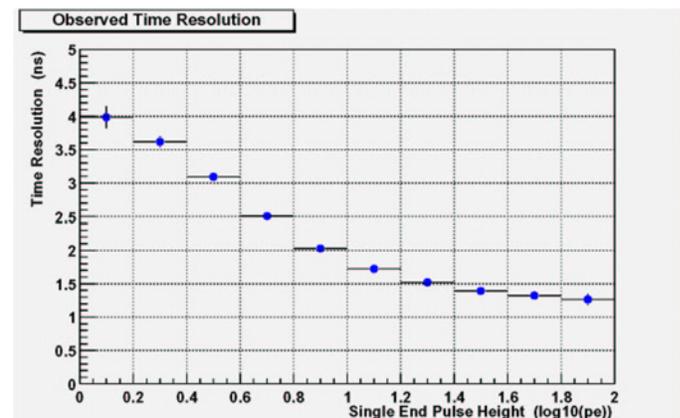


Fig. 5 Measured timing resolution vs pulse height

For each observed muon, the timing measurements are used to determine the signed velocity (normalized to the speed of light), where positive corresponds to downward going and negative to upward going.

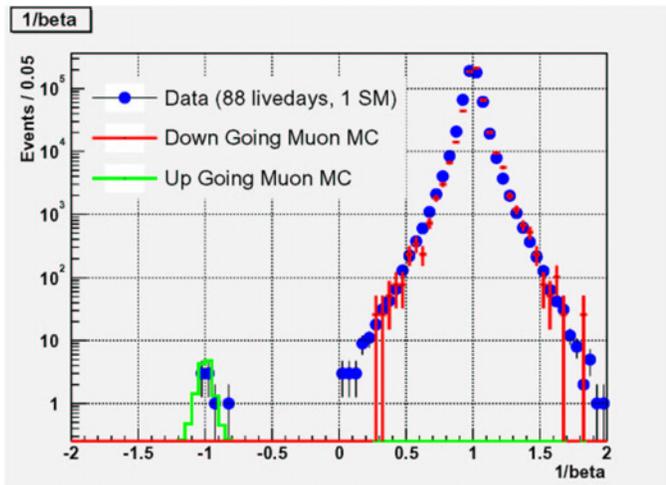


Fig. 6 Inverse velocity distributions

Fig. 6 shows the observed inverse velocity distribution for 88 days live-time for one super module (half the completed detector). The expected distributions from cosmic ray muons and from neutrino induced upward going muons are also shown^[7]. There is a well defined separation between the two types of events, validating the ability of the MINOS far detector to observe a clean sample of upward going muons.

¹ MINOS Technical Design Report

² ASD-lite, ATLAS Muon Spectrometer

³ MDT-ASD, ATLAS Muon Spectrometer

⁴ Quiet-Zone, Gore Cable Corp.

⁵ AD9240, Analog Devices Corp.

⁶ Xilinx

⁷ “Active detector simulation in gminos and reco_minos”
NuMI-NOTE-SIM-0479