



# **MINOS VARC**

## **Firmware Revisions**

N. Felt  
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## **1. ETC and Sparsifier 1.01**

### **1.1. Reset readout**

You no longer need to do a reset when changing modes. The only time you need to do a reset is when you initialize at power-up.

### **1.2. Automatic Cal-Inject**

The automatic Cal-Inject now works. The bit that selects automatic mode is no longer in the CAL\_TRIG\_XQT\_CTRL register; it is now bit 3 in the CONROL register. Writing a 1 to this bit will put the VARC in Automatic Triggerless-Pedestal or Automatic Cal-Inject mode, depending on bits [2:0]. While in Automatic Cal-Inject mode, the VARC will perform 1 cal-inject for every XQT it sees. In this mode you must have a VA chip installed for every VA chip enabled using the CHIP\_TRIG\_ENABLE Register. If a chip is enabled but not physically present the operation will get buggered up.

### **1.3. Error registers**

The ETC and Sparsifier now have error registers at 0x60 each bit will signal an error, which is described in the VARC document.

### **1.4. Revision Registers**

The Firmware revision registers now work. This number is set in the last byte of register 0x00 of all FPGAs on the board. The current version is 0x11 which means version 1, revision 01. In other words version 1.01

### **1.5. VME Buffer readout word**

The buffer readout word has been changed to include a VARC id. This two-bit value can be set in the first two bits of register 0x30 in the Sparsifier.

### **1.6. VMM analog cable connector**

In the previous version of the ETC, the bottom VMM connector corresponded to VFB 0, now VFB 0 should connect to the top VMM connector. There is no change to the gray ribbon cable connection. FEB 0 still connects to the right-hand connector.

## **2. Sparsifier 1.02**

### **2.1. Data corruption when changing modes**

Under certain circumstances when changing from cal-inject mode to a Triggerless-Pedestal mode the VME buffer became corrupt and required a reset. This has been fixed.

### **2.2. Sparsification**

Data sparsification has been improved.

### 2.3. Triggerless-pedestal mode

While the VARC is in Triggerless-pedestal mode, pedestal subtraction is automatically disabled.

## 3. ETC 1.03

### 3.1. Cal-inject trigger accept window

The automatic Cal-inject trigger accept window is adjusted.

### 3.2. Automatic Error Detection

The automatic error detection had been improved

### 3.3. Reset Readout

The ETCs reset automatically at power-up.

## 4. Master Clock 1.03

### 4.1. Base Address

The Base address will change with the new Master Clock firmware. The five most significant bits were wrongly inverted. This has been corrected. Using the MINOS crate, the first 9u slot is address 0x30 the second is 0x38 then 0x40. Use caution when using the first 9u slot because this might contain the LVDS terminating resistors on the J3 back plane.

### 4.2. Front Panel LED

There has been a change in the front panel LED to indicate the following situations.

|                |   |
|----------------|---|
| Solid Green    | Clock is generated from VARC  |
| Flashing Green | Clock is taken from clock module  |
| Amber          | VME Interaction   |
| Flashing Red   | An error has occurred. This is only reset by reading the error registers. |

## 5. ETC 1.04

### 5.1. Cal-inject charge delay

There is now a constant delay in the time between when the Cal-inject cap points to a VA channel and the time the charge is injected into the channel. This change will improve the results of the cal-injects for the lower numbered channels. This delay is set to 1280 VA readout clock periods. With a readout period of 250ns this will be 320us. This delay must be taken into account when figuring the maximum cal-inject rate. The rate is dependent on the VA clock period. With a 250ns readout period a rate of < 3 KHz should be safe.

## 5.2. Mode Changing Reset

When changing modes during a time when an extremely large (almost constant) rate of triggers are coming from the FEB the FIFO becomes out of sync. This is a very rare but possible problem. The reset sequence has been improved to fix this.

## 5.3. Reset during mode write

The ETC self resets whenever the mode is changed. The ETC will now self reset whenever the mode is written to, even if it is not changed.

## 6. Sparsifier 1.04

No changes have been made with this version.

The revision number on the Sparsifier reads 1.00 even though it is 1.04.

## 7. Master Clock 1.05

### 7.1. LEMO IO

The Board LEMO connector is connected to the Master clock FPGA. Using spare board connections we can route the LEMO signal to other chips on the board. The control register in the Master clock now controls whether the LEMO connector is an input or an output. If Bit1 is 0 then the LEMO is an output. If Bit1 is a 1 it can be used as an input.

## 8. ETC 1.06

### 8.1. Cal-inject Rate

Some protection was added to guard against a high rate of automatic cal-inject XQTs. Enough time should still be given to complete the cal-inject operation between XQTs; however, the crippling effects of a high XQT rate have been reduced.

### 8.2. Status bits

New Status bits are added.

## 9. Sparsifier 1.05

### 9.1. Net Label

In version 1.04 a net was mislabeled. In this unreleased version the pedestal memory does not properly work. This is corrected in this version.

### 9.2. Revision Register

The revision register now works in the Sparsifier too.

### 9.3. Errors Detection

New FIFO out of sync errors have been added to the Sparsifier. These errors will be reported in the error register. For more info see the users manual.

#### 9.4. Common mode correction

The common mode correction was changed to use channel 1,19,20,21 and not 18. The only alternative is to use 19,20,21,22 which can be done if people prefer.

#### 9.5. External triggers

Using the external LEMO configured in the Master Clock as an input, we can trigger a timestamp to be inserted into the output buffer. This is to be used for the Time of Flight data. This is an active low input signal.

To accommodate for this new functionality, bits needed to be changed in the control register. There used to be two bits required for the buffer test now it uses one. Bit0 is now the only bit needed to do the test. Bit2 is used to enable the external triggers.

### **10. Sparsifier 1.06**

#### 10.1. Error register

A new error has been added to the Sparsifier to indicate a VME read of a buffer that is currently being written to.

#### 10.2. Correction disable

The common mode correction, sparsification and pedestal subtraction are automatically disabled during cal-inject mode just as it is in the triggerless-pedestal mode.

### **11. Master Clock 1.06**

#### 11.1. Slow control

There is now manual control of the slow control lines on FEB 0 and 1. This feature will enable a test pattern to be generated with the software during FEB testing and will only be used when this aspect of the FEB is being tested. Manual controlled is enabled with bit 2 in the control register. The slow control bits can be toggled using register 0xbb100040. The bits are negative true.

Bit0 /Serial enable FEB0  
Bit1 /Serial enable FEB1  
Bit2 /Serial clock  
Bit3 /Serial data

For example, writing the values 0xA and 0xE toggle the Serial clock of FEB0.

#### 11.2. LED

The flash of the front panel LED is made to be more attractive.

## **12. ETC 1.07**

### **12.1. Bimodal Data**

A bimodal data problem was seen to be caused by charge on the data cable discharging through a transistor on the VMM when that VFB is deselected. This was fixed in the firmware by always switching to the VFB we are not interested in, thereby allowing its cable to charge up to a constant value. The VFB we intend to read out is then selected and we allow a short discharge time of the deselected cable. There this will cause some shift in the data but the shift will be constant and will be taken out with pedestal subtraction.

## **13. Mc1.08, ETC 3.02, Spars 2.04**

Both 2 of 6 and 2 of 36 triggers are in this version. See Trigger document for details.

## **14. Mc1.09, ETC 3.03, Spars 2.05 - 6/13/02**

This is a Cal-Det enabled version of the previous version. This version should not be used in a Soudan VARC.

The cal-injects are not working properly with this version.

## **15. Mc1.10 - 11/24/02**

The MC firmware was just recompiled for Soudan. The Master Clock *should* be functionally equivalent to 1.08.