

## **Coincidence Trigger**

In order to reduce the number of single uncorrelated FEB triggers being read-out, a coincidence trigger has been implemented in the VARC. This functionality resides in each ETC and is controlled using register 0x68. When this functionality is enabled, a trigger is accepted only if a trigger from a different VA chip is received within a selected time window. In other words, if two triggers occur within a set amount of time, both are read-out. There are 3 modes of coincidence trigger operation.

Because of PCB routing restrictions some functionality was removed to allow for this coincidence trigger. This removed functionality is the Event-Reducer and the Time-Of-Flight external trigger. These are things that should only effect the calibration detector. If firmware is upgraded at the calibration detector there is Cal-Det mode switch that must be enabled in the ETC, Sparsifier, and Master Clock firmware before it is compiled. This switch will replace the Coincidence trigger with the previous functionality.

### ***Disabled***

When this trigger is disabled, all FEB events are passed through the VARC to the DAQ. The trigger modes are disabled by setting the coincidence window to 0. These modes are automatically disabled whenever the VARC is not in run mode.

```
bb3e 0068 <= 0x X0
```

bb is the board address and e is the ETC number.

In this example we are disabling the coincidence trigger.

### ***2 of 6 trigger***

In this trigger mode, there needs to be a coincidence between a least two different VA chips in one ETC. Since each ETC only knows of 6 VA chips, this is a 2 out of 6 trigger. The coincidence window is set from 50 ns to 400 ns in steps of 25 ns using bits 3 down to 0 in register 0x68. Setting these bits to 0x0 corresponds to disabling the trigger modes. A value of 0x1 is 50 ns and a value of 0xF is 400ns. Bit 7 in register 0x68 is used to enable the 2 of 36 trigger and must be off in this mode. Register 0x68 must be properly set in all 6 ETCs.

```
bb3e 0068 <= 0x0F
```

In this example we are setting a 2 of 6 trigger with a coincidence window of 400 ns.

## ***2 of 36 trigger***

In this trigger mode, there needs to be a coincidence between a least two different VA chips in one VARC. Because of limitations in communication between ETCs, the coincidence window is fixed to be 475 ns +/- 10%. The coincidence window set using bits 3 down to 0 in register 0x68 should be set to 0xF. Bit 7 in register 0x68 is used to enable the 2 of 36 trigger and must be on in this mode. Also, each ETC must be told who he is using bits 6 down to 4 in register 0x68.

```
bb30 0068 <= 0x8F;  
bb31 0068 <= 0x9F;  
bb32 0068 <= 0xAF;  
bb33 0068 <= 0xBF;  
bb34 0068 <= 0xCF;  
bb35 0068 <= 0xDF;
```

In this example we are setting a 2 of 36 trigger.