



CalDet Timing System 2002

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Requirements



- All this is relevant for CalDet only !!!
- CalDet
 - FD: 2 read-out crates
 - ND: 1 read-out crate, several FE crates
 - ToF: 3 interfaced to FD electronics
 - Cerenkov: 1 interfaced to FD
- Simultaneous readout of of ND and FD electronics
 - DAQ: read out both electronics
 - Timing system: provide signals for both
 - physics: form events containing both types of hits



Requirements



- Start DAQ simultaneously
- Buffer swaps simultaneously
- ND and FD clock have to be translated into a real time to form snarls
- Snarls are formed in Trigger Farm containing both types of hits
- Solution:
 - Bad: two free running clocks with known frequency
 - Good: lock clocks and other timing signals together



FD Timing system



- System is based on 40 MHz clock
 - free running or
 - locked to GPS
- Timing signals provided
 - 40 MHz
 - 1 pps (counter reset, 1 Hz)
 - buffer swap (every 50 msec)
 - execute (trigger pedestal, charge injection,...)
- Distribution from 1 TCU or mTRC to 1-24 TRC
 - electrically (LVDS) or
 - optically



ND Timing System



- System is based on 53.1 MHz clock
 - free running or
 - locked to MI (main injector RF)
- Timing Signals
 - clock (53.1 MHz)
 - CNTRST (counter reset, < 2.68 sec)
 - SGATE (spill gate, probably not used at CalDet)
 - TBMKR (time block marker = buffer swap)
 - TCAL (QIE reset)
- Distribution from 1 master clock to all crates
 - electrically (LVDS)



Implementation



- Option A (FD Master)
 - FD TRC acts as master
 - sends signals to ND master clock (LVDS)
 - 1pps = CNTRST
 - 53.333 MHz signal locked to 40 MHz (simple 3:4 ratio)
 - buffer swap
 - calibration runs (TCAL, executes) independent
 - TCAL locked to 1pps (for QIE reset)
 - caveat
 - ND runs at 53.333 MHz, not 53.1 MHz
 - few oscillators change



Implementation (cont.)



- Option B (no Master)
 - ND time master sends signal to FD master TRC
 - clock (53.1 MHz)
 - FD master TRC locks
 - 40 MHz clock to 53.1 MHz
(optional on board VCXO , lock at 100 kHz)
 - FD mTRC sends to ND master
 - 1 pps
 - buffer swap
 - Caveat
 - more complicate
 - signals go back and forth
 - But both systems run at their real frequency



Implementation (cont.)



- Option C (ND master)
 - not possible
 - no inputs on TCU or mTRC for
 - buffer swap
 - boards already in production



Summary



- CalDet requires special timing system
- ND and FD have to be locked together
- Two similar possibilities do exist
 - Option A (FD master): simple
 - Option B (no master): preferred by Colin
 - Option C (ND master): impossible
- Draft note describing scenario in circulation